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Design and Performance Analysis of 4Kb SRAM Arrays Using 16nm GNRFET and CMOS with 1-Bit 6T Cells

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Abstract:

With the evolution in the microelectronic applications like high speed processors, multimedia and in current electronic communication for artificial intelligence devices and IOT necessitates bigger SOC SRAM arrays for high performance with low power consumption and less space. Generally, CMOS based technologies are most extensively utilised for the construction of 6T SRAM cell. When the nanoscale technology is scaling down CMOS devices are usually confronting with leakage current and short channel impact. The constant scaling of CMOS technology restricts the performance of 6T SRAM cell in terms of leakage power. Leakage current is the biggest contributor in the power consumption of SRAM. So, the researchers have invented GNRFET technology to compensate the CMOS technology. Graphene Nano Ribbon Field Effect Transistor is a three terminal device similar to MOSFET, here the semiconducting channel is created using graphene. In this study employing 1-bit 6T SRAM cell, 4kb memory array is developed using CMOS and GNRFET technologies at 16nm technology with supply voltage of 1v. Initially 4x4, 16x16, 32x32 SRAM arrays are created in two technologies and the parameter such as read delay, write delay and average power consumption are evaluated and the results are compared for the two technologies using HSPICE tool.

Keywords: SOC, SRAM, CMOS, GNRFET, MOSFET, HSPICE tool, read delay, write delay, average power.

1. INTRODUCTION

The organisation of embedded memory in current very large-scale integration (VLSI) systems has progressed to a more sophisticated level. Random access memory cells are generally divided into two types: static random-access memory (SRAM) cells and dynamic random-access memory (DRAM) cells. When compared to SRAM cells, which are implemented with transistors and latches, DRAM cells are implemented with capacitors and a single transistor, which takes a long time to charge and discharge the capacitors for storing and retrieving data, as well as consuming a significant amount of power during the process. Because of this benefit, SRAM cells are commonly employed in SOC devices which are semiconductor-based electronics [1].

As a result of the increasing need for power reduction and improved performance in modern SOC devices, several SRAM cells designs have been presented that are optimized for high performance. However, the 6T SRAM cell is often regarded as offering an excellent balance between size and performance. To boost performance, SOC devices make advantage of bigger SRAM arrays than are typically seen in other devices. Consequently, the effect on area resulting from the incorporation of a bigger SRAM array on the chip results in an indirect increase in power consumption, chip size, and cost [2]. When it comes to standard CMOS and GNRFET-based 16nm technology SRAM arrays, 1-bit 6T SRAM cells have been used to create them in the age of nanotechnology creation. The high-speed devices in extremely large-scale integrated circuits are becoming more prevalent as the size of the transistor's channel continue to reduce (VLSI). Because of the shrinking size of the transistor with each successive generation, the bulk CMOS technology has resulted in a continuous increase in the performance of contemporary digital circuits. In order to maintain the continuous scaling of bulk CMOS, considerable obstacles must be overcome owing to the underlying material and technological limitations of process technology. In order for the MOS transistor to work properly when its channel size approaches nanometers, leakage currents begin

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to cause abnormalities in its operation. Short Channel Effects are the term used to describe these functional abnormalities.

In order to comply with Moore's law, transistors must be scaled down in size. However, when the dimensions are reduced to nanometers, the short channel effect becomes superior, resulting in a trade-off between power dissipation and area [3]. The transistor leakage current is caused by the short channel effect, which is also caused by the short channel effect. As a consequence of this leakage current in the transistors, the power dissipation rises, and the transistor performance becomes less predictable. The search for an alternative device to CMOS devices has been conducted in order to avoid this trade-off while simultaneously ensuring the continuation of Moore's law [3, 4]. The graphene-based transistors are being employed as an alternate option for silicon-based transistors with scaled device geometry, according to the researchers.

Graphene is a carbon compound with a unique lattice type structure that has been discovered. Because carbon and silicon are members of the same group in the periodic table, some of the characteristics of graphene are comparable to those of silicon, which is a good thing. A honeycomb-like structure is formed by the carbon atoms in graphene, which is composed of carbon atoms packed densely together. Graphene, in its most basic form, is a conductor with a zero band-gap. The semiconducting quality of the material used to construct the transistor is essential. In order to convert Graphene into a semiconducting material, a band-gap must be created in the material's structure. Processed graphene sheets are converted into graphene nano ribbons (GNRS), which are used in many applications. When the GNR is narrowed, the band-gap shrinks, and this is inversely proportional to the width of the GNR [4]. In order to create GNRFETs, GNR is employed as a channel material in transistors, similar to how silicon is used.

Using the HSPICE tool in both CMOS and GNRFET technologies, the article tries to construct a 4KB memory array. It is possible to develop and implement peripherals in two different technologies, such as the row decoder, the column decoder, the write driver circuit, the control circuitry, the pre-charge circuit, and the sensing amplifier. The project's goal is to successfully develop a low-power memory array and show that it can perform both write and read operations. The following is the structure of this paper: Section 2 provides an overview of CMOS and GNRFET technology. The SRAM array architecture is discussed in Section 3. The design and implementation of an SRAM array are discussed in Section 4. The comparative examination of SRAM arrays is presented in Section 5. Section-6 concludes the paper's discussion of its main points.

2. REVIEW OF CMOS AND GNRFET

Since the 1970s, CMOS technology has been scaling down from one technology node to the next in order to enhance the performance and size of semiconductor integrated circuits (SOCs). The SRAM cell is a critical component of SOC devices' integrated memory. For the most part, because of its rapid response time, SRAM is employed as a cache memory in microprocessors. When it comes to sophisticated microprocessors, leakage power is the most significant cause of power dissipation in the microprocessor [5]. When it comes to reducing leakage power in the cache memory, scaling is one of the solutions available to the semiconductor industry, which is primarily reliant on MOSFETs for their operation. Because of basic material and process technology limitations, the continual scaling of CMOS transistors will meet hurdles in the future, including the short channel effect and other severe challenges in the near future. Therefore, it is necessary to replace the silicon material with other materials to get the desired results. Because of the superior capabilities of graphene material, graphene-based semiconducting materials are being considered as a potential replacement for silicon-based semiconducting materials in devices with scaled device geometry.

The graphene-based field-effect transistor (GNRFET) is one of the graphene-based transistors that may be used to replace standard silicon transistors in scaled technologies [6]. When fabricating a GNRFET, graphene nano ribbons (GNRs) are employed as the channel material. Due to the use of graphene as a material, GNRFET devices are very tiny, and the range in circuit performance is quite great when compared to silicon-based devices. Multiple graphene nano ribbons (GNRs) are joined in parallel to produce extensive conducting contacts in a single graphene nano ribbon field-effect transistor (GNRFET). Patterning is used to control the width of the GNRs (g), and the distance between the ribbons (gs) is used to maintain the spacing between them.

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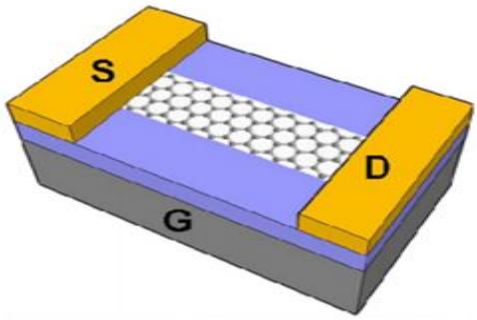

Figure 1a: Structure of a GNRFET

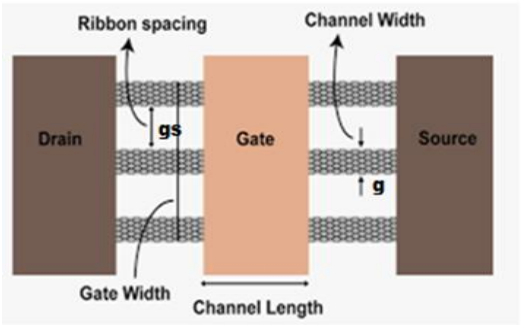

Figure 1b: Cross sectional view of a GNRFET

The width of the GNRFET is determined by the number of dimmer lines present [6]. A general-purpose GNRFET may be divided into two types: the Metal Oxide Semiconductor (MOS) type GNRFET and the Schottky Barrier (SB) type GNRFET. The MOS-GNRFET has source and drain terminals that are connected to the GNR intrinsic channel [6]. Similarly, the SB-GNRFET has a GNR intrinsic channel as well, however the source and drain terminals are composed of metal instead of plastic. When compared to SB-GNRFETs, MOS-GNRFETs have a greater ION/IOFF ratio [12]. The MOS type GNRFET is chosen in the design of the 6T-SRAM cell because the MOS-like structure offers various benefits over the Schottky barrier type MOSFET [13] in terms of performance. The key benefit over the SB GNRFET is the larger ION/IOFF current ratio, higher transconductance, and quicker switching speed, which results in a decreased latency during the write and read operations [14]. GNRs are manufactured using a variety of manufacturing processes, including lithography [7], chemical synthesis [8], and unzipping from carbon nanotubes [9].

3. SRAM ARRAY ARCHITECTURE

The architecture of the SRAM array is discussed in detail in this section. The basic SRAM array construction is shown in the following Figure 2 [14].

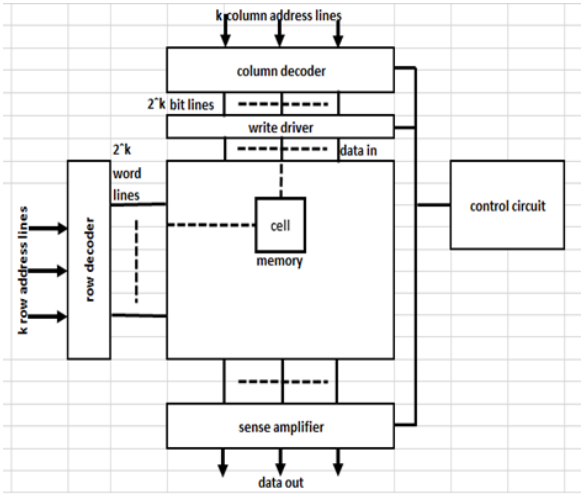

Figure 2: General structure of SRAM array

SRAM arrays may be structured in one of two ways, depending on the requirements. There are two ways to organize data: one as bit-oriented organisation and the other as word-oriented organisation. SRAM is organized in a bit-oriented manner, with each address accessing a single bit of data. With contrast, in the word-oriented architecture of SRAM, each address corresponds to a word containing n-data bits [10].
Using a column decoder or column mux that is addressed by the 'K' address bits, a single sense amplifier may be shared across two, four, or more columns in a word-oriented organisation. A single sense amplifier is shared by one column in the bit-oriented design, which allows for a more thorough read process [10].

An SRAM cell must be constructed in such a manner that it can perform both a reliable writing operation and a non-destructive read operation without causing damage to the device. With these two needs in mind, the transistor sizing in the SRAM cell must be done in order to achieve effective read and write operations.

4. DESIGN AND IMPLEMENTATION OF SRAM ARRAY

The purpose of this part is to explore the design and implementation of a 4Kb SRAM array in a bit-oriented organisational structure. The fundamental construction of an SRAM array is comprised of a 1-bit 6T SRAM cell, write driver circuits, a pre-charge circuit, an isolator circuit, a sense amplifier, and row and column decoders,

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among other components. Figure 3 depicts the fundamental implementation of an array of elements.

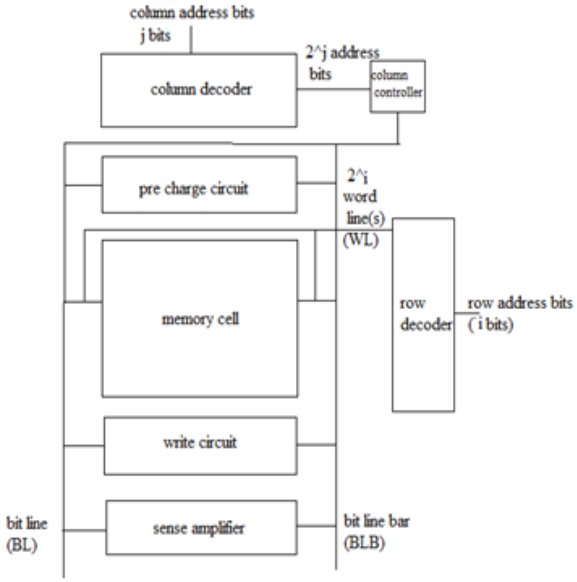

Figure 3: Basic implementation of SRAM array

4.1 Design of l-bit 6T SRAM cell

In this paper, the 6T SRAM cell is developed in both CMOS and GNRFET technologies, with the CMOS design taking precedence. The basic structure of an SRAM cell consists of two cross couple inverters, which serve as the memory cell, and two NMOS transistors, M5 and M6, which serve as access transistors (pass transistors), and which are connected to the memory cell's output nodes as well as to the outside world via the bit line (BL) and the bit line bar, respectively (BLB). The word line (WL) at the gate terminal of access transistors allows the memory cell to function in a variety of different modes of operation.

4.1.1 Design of 6T SRAM cell in CMOS technology

Figure 4 depicts a 6T SRAM cell in CMOS technology, which corresponds to the explanation in Section 3 of this paper. To achieve a non-destructive read operation as well as a reliable write operation, the 6T SRAM cell is built with a cell ratio (CR) more than 1 and a pull up ratio (PR) less than 1, as described in [11].

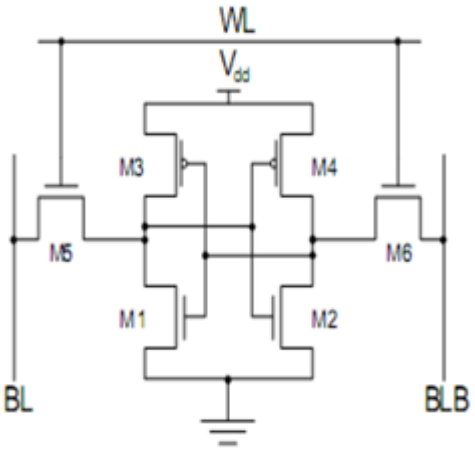

Figure 4: 6T SRAM cell in CMOS technology

Cell ratio (CR) = (W_M1/L_M1) / (W_M5/L_M5) (during read operation)
Pull up ratio (PR) = (W_M4/L_M4)/(W_M6/L_M6) (during write operation)

4.1.2 Design of 6T SRAM cell in GNRFET technology

This section of the study involves the design of a 6T SRAM cell, which is seen in figure 5. A MOS-type GNRFET is used in this section. However, as mentioned in Section 2, although the circuit architecture is identical to that of a CMOS-based 6T SRAM, the channel of the GNRFET is made of graphene material. The performance of the cell is determined by the quantity of ribbons present in each transistor.

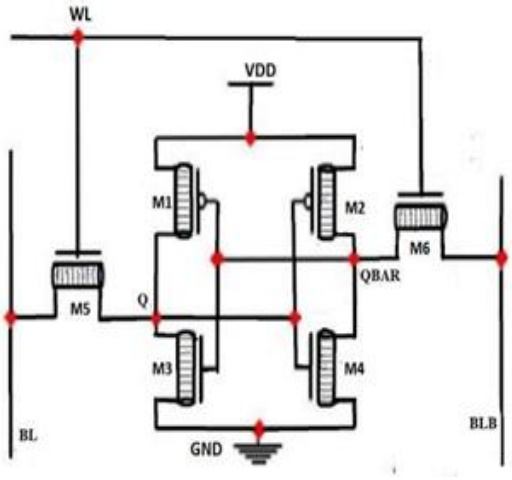

Figure 5: 6T SRAM cell in GNRFET technology

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The design parameters used for GNRFET technology are N: 6, Tox: 0.6nm, dop: 0.001, L:16nm, Tox2:20nm and nRib:6 for pull up transistors, 12 for pull down transistors and 8 for access transistors.

4.2 Operation of SRAM cell

During both read and write operations, the access transistors are enabled by driving the word line high, which allows for activation of the SRAM cell. The write driver circuit consists of a straightforward tristate buffer. Tristate buffer is linked to each bit line of the memory cell in the array via the tristate buffer. The enable signal of the buffer serves as a write enable (WE) signal for the purpose of performing a write operation on the buffer. The buffer's input is linked to the data signal (DATA), and its output is connected to the bit lines (BL, BLB) of the memory cell, allowing the data to be imposed in the memory cell via the buffer.

The write operation of an SRAM cell is determined by the data in the following Table 1.

Table 1: Operation of write circuit

WE	DATA	Operation
0	x	M1, M2 are OFF, path exit. No operation
1	0	M1, M2 are ON, path exist. Operation done, M6 ON, bit line (BL) of the memory cell is imposed with bit'0' and M7 ON, bit line bar (BLB) is imposed with bit '1'
1	1	M1, M2 are ON, path exist. Operation done, M5 ON, bit line (BL) of the memory cell is imposed with bit'1' and M8 ON, bit line bar (BLB) is imposed with bit '0'

The pre charge circuit consists of a basic column pull-up transistor that is coupled to each of the memory cell's bit lines (BL and BLB). Both bit lines (BL and BLB) are pulled to supply voltage during the read operation, causing both bit lines to be treated in the same manner. Predicting the gate terminal of the pull up transistor (PMOS) is accomplished via the use of the control signal "PRE." The project makes use of a sense amplifier of the latch kind. As with a 6T SRAM cell, this sort of sense amplifier is composed of a pair of cross-coupled inverters that work together. Because the latch type sense amplifier does not provide isolation between the inputs and outputs, an isolator circuit is necessary. The isolator aids in the isolation of the sense amplifier's input and output bit lines (BL and BLB), respectively. A certain voltage differential between two-bit lines (BL, BLB) causes the control signal 'SE' to be activated, which isolates the SRAM cell and sense amplifier bit lines (BL, BLB), with the voltage on the bit line being monitored by a sense amplifier.

4.2.1 Row and column decoder

The design of the row and column decoders with the control signals is based on a straightforward and fundamental 'and gate' based decoder. A 6:64 row and column decoder for the 4kB SRAM array is developed using the finest structure possible, as seen in the truth table.

The row and column decoders are one of the most significant peripherals in the architecture of an SRAM array since they provide access to the memory cells. In order to access the 4Kb SRAM array, a 6:64 decoder is necessary. When the row decoder produces an output, it is used to access the word line of memory cells for each row of the SRAM array, and when the column decoder produces an output, it is used to choose the specific column of the SRAM array to be accessed for mode of operations. The 6:64 decoder has six inputs as well as one control signal to work with. Following the mode of operation, the control signal of the row decoder and column decoder deactivated the word line and column selection signals of the SRAM cell, resulting in an indirect reduction in the power consumption of the memory cell.

Using a 6:64 decoder, which picks particular word lines (word) and column selections (cs) for the matching row and column of a 4Kb SRAM array, the outputs shown in Table 2 are shown below.

Table 2: (a)&(b) 6:64 row and column decoder with output selection

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Inputs							Output
en/cen	i1/j1	i2/j2	i3/j3	i4/j4	i5/j5	i6/j6	word/cs
0	x	x	x	x	X	x	X
1	0	0	0	0	0	0	1
1	0	0	0	0	0	1	2
1	0	0	0	0	1	0	3
1	0	0	0	0	1	1	4
1	0	0	0	1	0	0	5
1	0	0	0	1	0	1	6
1	0	0	0	1	1	0	7
1	0	0	0	1	1	1	8
1	0	0	1	0	0	0	9
1	0	0	1	0	0	1	10
1	0	0	1	0	1	0	11
1	0	0	1	0	1	1	12
1	0	0	1	1	0	0	13
1	0	0	1	1	0	1	14
1	0	0	1	1	1	0	15
1	0	0	1	1	1	1	16
1	0	1	0	0	0	0	17
1	0	1	0	0	0	1	18
1	0	1	0	0	1	0	19
1	0	1	0	0	1	1	20
1	0	1	0	1	0	0	21
1	0	1	0	1	0	1	22
1	0	1	0	1	1	0	23
1	0	1	0	1	1	1	24
1	0	1	1	0	0	0	25
1	0	1	1	0	0	1	26
1	0	1	1	0	1	0	27

(a)

en/cen	i1/j1	i2/j2	i3/j3	i4/j4	i5/j5	i6/j6	word/cs
1	1	0	0	0	0	0	33
1	1	0	0	0	0	1	34
1	1	0	0	0	1	0	35
1	1	0	0	0	1	1	36
1	1	0	0	1	0	0	37
1	1	0	0	1	0	1	38
1	1	0	0	1	1	0	39
1	1	0	0	1	1	1	40
1	1	0	1	0	0	0	41
1	1	0	1	0	0	1	42
1	1	0	1	0	1	0	43
1	1	0	1	0	1	1	44
1	1	0	1	1	0	0	45
1	1	0	1	1	0	1	46
1	1	0	1	1	1	0	47
1	1	0	1	1	1	1	48
1	1	1	0	0	0	0	49
1	1	1	0	0	0	1	50
1	1	1	0	0	1	0	51
1	1	1	0	0	1	1	52
1	1	1	0	1	0	0	53
1	1	1	0	1	0	1	54
1	1	1	0	1	1	0	55
1	1	1	0	1	1	1	56
1	1	1	1	0	0	0	57
1	1	1	1	0	0	1	58
1	1	1	1	0	1	0	59
1	1	1	1	0	1	1	60
1	1	1	1	1	0	0	61
1	1	1	1	1	0	1	62
1	1	1	1	1	1	0	63
1	1	1	1	1	1	1	64

(b)

The SRAM array has a capacity of 4096 bits thanks to the use of a 6:64 row and column decoder combination, respectively. Image 3 depicts an SRAM array with 4096 6T SRAM cells. Each column of the array has three components: a write circuit, a pre charge circuit, and a sense amplifier, all of which are illustrated in the figure. The readout signals on the 4Kb SRAM array total 64 in number. The word line is accessed using the inputs i1, i2, i3, i4, i5, and i6 of the row decoder in order to perform read and write operations on the selected cell, which is determined by the inputs j1, j2, j3, j4, j5, and j6 of the column decoder in order to perform read and write operations on the selected cell.

5. COMPARITIVE ANALYSIS OF SRAM ARRAY

This section describes the comparative study of a 4KB SRAM array that was constructed using CMOS and GNRFET based technologies, respectively. Using the Synopsys HSPICE programme, these

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designs are simulated at 16 nm technologies with a 1V supply, and the performance parameter values of read delay, write delay, power dissipation, and average powers are given in Table 3. As a starting point, a 1-bit 6T SRAM cell is developed in both CMOS and GNRFET technologies at 16nm technology, and the performance characteristics for each of these designs are estimated using the HSPICE tool. Subsequently, SRAM arrays of different sizes (e.g., 4x4, 8x8, 16x16, 32x32) are constructed to confirm the findings achieved with the 4Kb SRAM array.

5.1 SIMULATION RESULTS

5.1.1 Simulation results of 64x64 SRAM array

The simulation results of 64x64 SRAM array with data input '1' and data input'2' are shown in Figure 15.

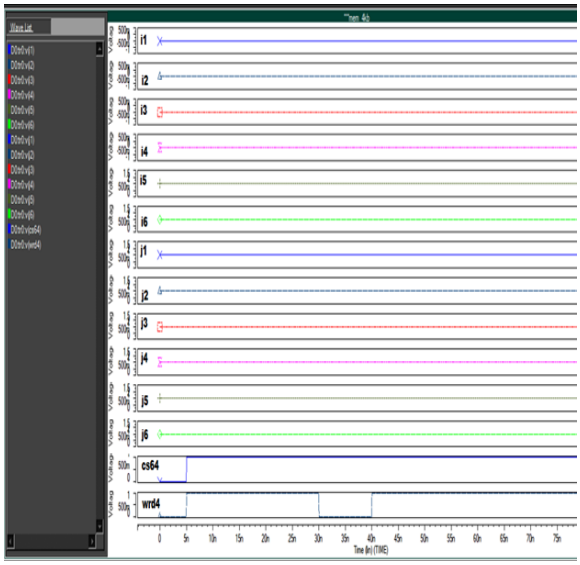

Figure 15.a Simulation results of row and column address selection of 64x64 SRAM

The row and column address signals of a 64x64 static random access memory array are determined by the signals i1, i2, i3, i4, i5, i6, j1, j2, j3, j4, j5, and j6 (000011111111) in the transient response shown in the preceding figure. The first six signals represent row address selection (i1, i2, i3, i4, i5, i6) signals and the next six signals represent column address selection (j1, j2, j3, j4, j5, j6) signals. Cs64 and word4 are the column and row selection signals of the memory array, respectively, that are used to identify the chosen memory cell (256) in relation to the previously specified row and column addresses.

The transient response of a 64x64 SRAM array with logic '1' and logic '0' is depicted in Figures 15.b and 15.c, where the associated 6T SRAM cell is picked to execute the read and write operations based on the row (wrd) and column (cs) address selection.

As previously stated in the preceding paragraph, the logic 1 and 0 are stored in a chosen memory cell (256), with the row and column addresses being picked as indicated in Figure 15.b and Figure 15.c below.

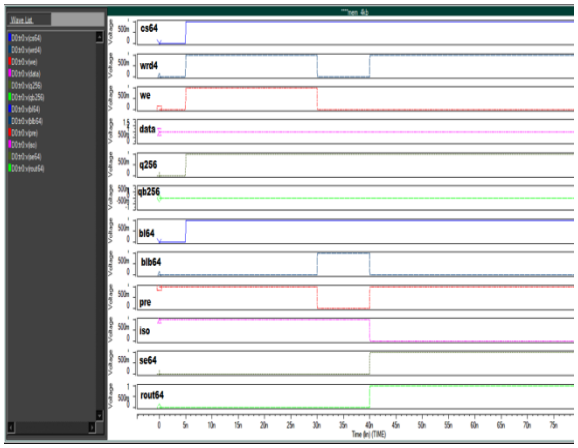

Figure 15.b: Logic 1 simulation results of 64x64 SRAM array

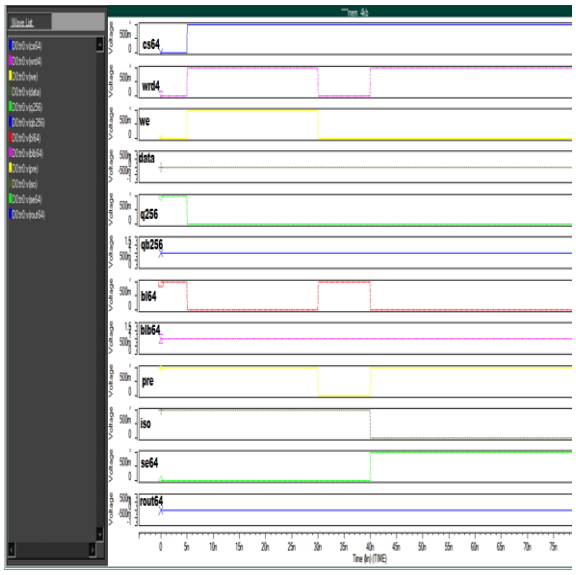

Figure 15.c: Logic 0 simulation results of 64x64 SRAM

The result seen above indicates that the write and read operations on the 64x64 SRAM array were completed successfully. The data signal is denoted by

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Table 3: Comparative analysis of SRAM arrays in CMOS and GNRFET technologies

PARAMETERS	Power dissipation (watts)	Average power (watts)	Read delay (seconds)	Write delay (seconds)

the symbol 'DATA'. The write enable signal is represented by the letter 'WE'. 'PRE' stands for pre-charge signal. The sense enable signal of the sense amplifier is represented by SE64, and the data out signal from the chosen memory array is represented by Rout64.

5.2 Comparative analysis of SRAM arrays in CMOS and GNRFET technologies.

5.2.1: Design parameters of CMOS and GNRFET.

The transistor sizing of the SRAM cell is critical for achieving proper functionality of the memory cell during the write and read operations. The transistor sizing plays a vital role for obtaining nondestructive readout data of the stored cell during the read operation and for storing the data in the memory cell by modifying the data of the stored cell during the write operation. The dimensions specifications of the SRAM cell are taken into consideration while sizing the transistors of the memory cell in order to achieve non-disruptive operations throughout the design process.

The dimensional parameters of the CMOS and GNRFET are listed in the below Table 2.

Table 2: Dimensional parameters of CMOS and GNRFET technologies

PARAMETERS	TECHNOLOGY/ DEVICES		
	CMOS		
	PMOS	NMOS	ACCESS TRANSISTORS
CHANNEL LENGTH (L)	0.016u	0.016u	0.016u
CHANNEL WIDTH (w)	0.016u	0.032u	0.018u
NO OF RIBBONS (nRib)	GNRFET		
	6	12	8

CMOS 6T SRAM cell design is discussed in this work, with the cell ratio '1.6' and pull up ratio '0.8' being taken into consideration. When designing a GNRFET 6T SRAM cell, the cell ratio of 1.5 and the pull up ratio of 0.75 are taken into consideration.

5.2.2: Comparative analysis of SRAM arrays in CMOS and GNRFET technologies:

According to Table 3, the various bit-oriented SRAM arrays parameter analysis report is stated from 1-bit cell to 64x64 SRAM array. The 1-bit memory cell in GNRFET technology uses 98 percent less power than the 1-bit memory cell in CMOS technology.

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TECHNOLOGY	CMOS	GNRFET	CMOS	GNRFET	CMOS	GNRFET	CMOS	GNRFET
1-bit SRAM cell	4.13E-08	2.09E-08	5.67E-06	7.30E-08	6.56E-08	4.09E-11	5.14E-09	7.39E-12
4x4 SRAM Array	7.2592-06	1.51E-07	1.56E-05	2.38E-07	1.20E-07	9.05E-11	1.31E-08	1.75E-11
8X8 SRAM Array	11.4832-06	2.17E-07	4.66E-05	3.61E-06	2.80E-07	1.99E-10	4.01E-08	2.34E-11
16X16 SRAM array	28.9565-06	3.37E-07	8.24E-05	1.13E-05	6.56E-07	5.90E-10	6.63E-08	3.25E-11
32X32 SRAM array	89.6114-06	7.80E-06	1.56E-04	1.53E-05	7.30E-07	6.90E-10	7.96E-08	4.99E-11
64X64 SRAM array	336.966-06	2.37E-06	5.47E-04	3.91E-05	9.94E-07	7.94E-10	9.05E-08	6.22E-11

The access time of the memory cell in GNRFET technology is 37 percent quicker in read mode and 85 percent faster in write mode than the access time of the memory cell in CMOS technology.

It also demonstrates that the access time of a memory cell in GNRFET technology is quicker than the access time of a memory cell in CMOS technology while performing read and write operations on a chosen memory cell in an array of memory.

Write delay in GNRFET technology is 93 percent less than the CMOS technology in the 64x64 array, while read delay in GNRFET technology is 93 percent less than the CMOS technology in the 64x64 array. The power consumption is on average 92 percent lower than that of the CMOS technology. The GNRFET-based array outperforms the CMOS-based array in terms of speed.

Finally, the table is stating that the GNRFET technology-based SRAM arrays are better than the CMOS technology.

6. CONCLUSION:

This paper contains the design and analysis of 64x64 SRAM array in bit orientation in CMOS and GNRFET technologies. It gives an answer to the rising need for larger memory capacity with reducing power consumption and access time with the analysis report stated in Table3. The design of SRAM array is simulated with supply voltage of 1volts at 16nm technology using Synopsys HSPICE tool. A 1-bit 6T SRAM cell based on CMOS and GNRFET technology has been built and tested. Then, using

CMOS and GNRFET technologies, all of the sub-blocks, including the 1-bit 6T SRAM cell, write driver circuit, pre-charge circuit, row and column decoders, and sensing amplifier, are developed and built in HSPICE. The inbuilt memory has a capacity of 4096 bits and is divided into 64x64 blocks. Multiple SRAM arrays are used to compare the performance of various performance characteristics such as power dissipation, average power, read and write access time, and so on. When compared to CMOS technology, the GNRFET technology dissipates 92 percent less power and operates at a quicker rate than the CMOS technology on an average.

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